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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/524,749	02/15/2005	Hiroyuki Yoshida	09792909-6113	6915

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EXAMINER	
KALAM, ABUL	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/524,749	YOSHIDA, HIROYUKI	
	Examiner	Art Unit	
	Abul Kalam	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) *1-3 and 6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4,5 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/15/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Election/Restrictions

Applicant's election without traverse of Group II, claims 4-5 and 7, in the reply filed on May 12, 2006 is acknowledged. Thereby claims 1-3 and 6 are withdrawn from further consideration for being drawn to a non-elected invention.

Claim Objections

1. Claim 5 is objected to because of an antecedent basis issue. The limitation "a method of manufacturing an insulated gate field effect transistor," in lines 1-2 of claim 5, should be amended to "The method of manufacturing..." in order to provide proper antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Roche (US 6,630,719).

With respect to claim 4, Roche teaches a method of manufacturing an insulated gate field effect transistor (N1) having a gate electrode (2) on a substrate with a gate insulating film interposed between said substrate and said gate electrode (col. 2, lns.

60-67), and having a source region and a drain region (3 and 4) formed in said substrate on both sides of said gate electrode (col. 3, lns. 1-2), said method comprising:

a step for forming in advance a first diffusion layer (11) of a first conduction type (p-type) in said substrate at a position deeper than a region where said source region and said drain region are formed in said substrate; and

a step for forming in advance a second diffusion layer (10) of the first conduction type having a higher concentration (P+) than said first diffusion layer (P-) and formed in said substrate at a position deeper than said first diffusion layer (fig. 1, col. 3, lns. 31-41).

3. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Taguchi et al. (US 5,220,190).

With respect to claim 4, Taguchi teaches a method of manufacturing an insulated gate field effect transistor (fig. 1, "N-channel MOSFET") having a gate electrode (50_3, fig. 4F) on a substrate with a gate insulating film (48) interposed between said substrate and said gate electrode, and having a source region and a drain region (58_3, fig. 4I) formed in said substrate on both sides of said gate electrode, said method comprising:

a step for forming in advance a first diffusion layer (24, fig. 4D) of a first conduction type (p-type) in said substrate at a position deeper than a region where said source region and said drain region are formed in said substrate; and

a step for forming in advance a second diffusion layer (40, fig. 4C) of the first conduction type having a higher concentration (P+) than said first diffusion layer (col. 7,

lns. 28-39) and formed in said substrate at a position deeper than said first diffusion layer (figs. 4A-4J, col. 4, lns. 38-67; col. 5, lns. 1-67; col. 6, lns. 1-67; col. 7, lns. 1-27).

4. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (US 6,023,293).

With respect to claim 4, Watanabe teaches a method of manufacturing an insulated gate field effect transistor (figs. 2, 16, and 17) having a gate electrode (22) on a substrate with a gate insulating film (27) interposed between said substrate and said gate electrode (col. 3, lns. 55-58), and having a source region and a drain region (25 and 26) formed in said substrate on both sides of said gate electrode (col. 3, lns. 58-64), said method comprising:

a step for forming in advance a first diffusion layer (21, fig. 2) of a first conduction type (p-type) in said substrate at a position deeper than a region where said source region and said drain region are formed in said substrate; and

a step for forming in advance a second diffusion layer (110, fig. 2) of the first conduction type having a higher concentration (P+) than said first diffusion layer (P-) and formed in said substrate at a position deeper than said first diffusion layer (col. 13, lns. 15-65).

With respect to claim 5, Watanabe teaches the method of manufacturing an insulated gate field effect transistor, as set forth above in claim 4 above, wherein a diffusion layer (24, fig. 2) of an N type is formed in advance in a region between said

source region and said drain region formed in said substrate with a region of said substrate ("well separation portion C") left on a surface side of said substrate.

With respect to claim 7, Watanabe teaches a method of manufacturing an image pickup device (figs, 2, 16, and 17) in which a part or all of insulated gate field effect transistors form an output circuit in the image pickup device and are formed in a substrate, said method comprising:

a step for forming in advance a first diffusion layer (21, fig. 2) of a first conduction type (p-type) in said substrate where said insulated gate field effect transistors are formed, at a position deeper than a region where a source region and a drain region (25 and 26) of said insulated gate field effect transistors are formed; and

a step for forming in advance a second diffusion layer (110) of the first conduction type having a higher concentration (P+) than said first diffusion layer (P-) in said substrate at a position deeper than said first diffusion layer (col. 13, lns. 15-65).

5. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Miida (US 6,051,857)

With respect to claim 4, Miida teaches a method of manufacturing an insulated gate field effect transistor (figs. 3) having a gate electrode (19) on a substrate with a gate insulating film (18) interposed between said substrate and said gate electrode (col. 3, lns. 55-58), and having a source region and a drain region (16 and 17a) formed in

said substrate on both sides of said gate electrode (col. 9, lns. 8-20), said method comprising:

a step for forming in advance a first diffusion layer (15) of a first conduction type (p-type) in said substrate at a position deeper than a region where said source region and said drain region are formed in said substrate; and

a step for forming in advance a second diffusion layer (11) of the first conduction type having a higher concentration (P+) than said first diffusion layer and formed in said substrate at a position deeper than said first diffusion layer (fig. 3).

With respect to claim 5, Miida teaches the method of manufacturing an insulated gate field effect transistor, as set forth above in claim 4 above, wherein a diffusion layer (15a) of an N type is formed in advance in a region between said source region and said drain region formed in said substrate with a region (between 17a and 14) of said substrate left on a surface side of said substrate (col. 8, lns. 51-53; col. 9, 29-34).

With respect to claim 7, Miida teaches a method of manufacturing an image pickup device (fig. 6) in which a part or all of insulated gate field effect transistors form an output circuit in the image pickup device and are formed in a substrate, said method comprising:

a step for forming in advance a first diffusion layer (15) of a first conduction type (p-type) in said substrate where said insulated gate field effect transistors (fig. 6) are formed, at a position deeper than a region where a source region and a drain region (16 and 17a) of said insulated gate field effect transistors are formed; and

a step for forming in advance a second diffusion layer (11) of the first conduction type having a higher concentration (P+) than said first diffusion layer in said substrate at a position deeper than said first diffusion layer (fig. 6).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abul Kalam whose telephone number is 571-272-8346. The examiner can normally be reached on Monday - Friday, 9 AM - 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abul Kalam

ANH D. MAI
PRIMARY EXAMINER